UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/032,863	03/02/1998	GORDON F. GRIGOR	0100.01117	1397

23418 7590 04/22/2003

VEDDER PRICE KAUFMAN & KAMMHOLZ
222 N. LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
NGUYEN, KEVIN M	
ART UNIT	PAPER NUMBER
2674	30

DATE MAILED: 04/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/032,863	GRIGOR ET AL.	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	DO

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24,29-33,38-54 and 56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24,29-33,38-53 and 56* is/are rejected.

7)☒ Claim(s) *54* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 12th, 2003 has been entered. An action on the RCE follows:

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 33 and 38-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Regarding claims 33 and 38-41, the word "means" is preceded by the word(s) "storing programming instructions" in an attempt to use a "means" clause to recite a claim element as a means for performing a specified function. However, since no function is specified by the word(s) preceding "means," it is impossible to determine the equivalents of the element, as required by 35 U.S.C. 112, sixth paragraph. See *Ex parte Klumb*, 159 USPQ 694 (Bd. App. 1967).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 24, 29, 31-33, 38, 40-46, 48-52 and 56 are rejected under 35 U.S.C. 102(b) as being anticipated by Zenda (US 4,980,678) hereinafter Zenda '678.

7. *As to claim 24*, Zenda '678 teaches a video graphics processing circuit comprising: a central processing unit (CPU) (1); and

a set-up RAM 24 and a PD setting control circuit 29 operably coupled to the CPU (1), wherein the set-up RAM 24 and the PD setting control circuit 29 store programming instructions that, when executed by a CPU 1, cause a D-flip flop 59 of the CPU 1 to (a) receive display preferences regarding two display CRT 19 and PDP 21 (figure 8);

(b) determine whether the display preferences can be fulfilled in observance of at least one of : configuration properties of the two displays (CRT 19 and PDP 21) and configuration properties of a computing system, the D-flip flop 59 determining whether a current configuration of two displays CRT 19 and PDP 21 to the computing system can be reconfigured such that the display preferences can be fulfilled while maintaining effective configuration of the current configuration when the display preferences cannot be fulfilled;

(c) configure the computing system and two displays CRT 19 and PDP 21 in accordance with the display preferences when the display preferences can be fulfilled,

and reconfigure operable coupling of the multiple displays to the computing system such that two displays CRT 19 and PDP 21 are configured in accordance with the display preferences when the current configuration can be reconfigured (see figure 11A and 11B);

(d) a coupling controller (D flip-flop 59) of the CPU (1) to operably couple a CRT controller 12 of a computing system to two displays (CRT 19 and PDP 21), a CRT controller 12 and PDP 14 providing display data to two displays (CRT 19 and PDP 21) (see figure 8);

(e) the D-flip flop 59 of the CPU (1) to operably couple the CRT controller 25 to a plurality of bits V-RAM 15, each of the plurality of bits V-RAM 15 and the CRT controller 25 storing separate display data and the CRT control 25 retrieving the display data from the plurality of bits V-RAM 15; and (see figure 8);

(f) a D-flip flop 59 of the CPU (1) to operably couple the CRT controller 12 and PDP controller 14 to a display driver CRT (19) and PDP (21), each of display driver CRT (19) and PDP (21) writing the separate display data to the plurality of bits V-RAM 15 (see figure 8).

As to claim 29, Zenda '678 teaches a video graphics processing circuit having a first display controller 12 coupling a first display CRT 19 and a second display controller 14 coupling a second PDP 19 (figure 8);

As to claims 31 and 32, Zenda '678 teaches a digital storage medium having at least two display controller 12 and 14 coupling to one screen memory (V-RAM 15) (figure 8).

8. *As to claim 33*, Zenda '678 teaches a digital storage medium for storing programming instructions that, when executed by a CPU (1), cause the CPU 1 to configure CRT 19 and PDP associated with a computing system, a digital storage medium (figure 8) having a coupling controller (D flip-flop 59) performs:

the first means for storing programming instructions (decoder 61) that cause a coupling controller (D flip-flop 59) to receive display preferences regarding two displays (CRT 19 and PDP 21) (column 6, lines 25-53);

the second means... to determine whether the display preferences (user selections) can be fulfilled in observance of at least one of: configuration properties (refresh rate or resolution) of two displays (CRT 19 and PDP 21) and configuration properties of the computing system (see column 7, lines 49-68);

the third means...to configure the computing system and the multiple displays in accordance with the display preferences when the display preferences can be fulfilled;

a digital storage medium (figure 8) having a CPU 1 performs fourth means:

determine whether a current configuration of two displays (CRT 19 and PDP 21) to the computing system can be reconfigured such that the display preferences can be fulfilled while maintaining effective configuration of the current configuration when the display preferences can not be fulfilled;

reconfigure operable coupling of the multiple displays to the computing system such that the multiple displays are configured in accordance with the display preferences when the current configuration can be reconfigured;

operably couple a CRT controller 25 of the computing system to the two displays (CRT 19 and PDP 21), the CRT controller 25 providing display data to CRT 19 and PDP 21;

operably couple the CRT controller 25 to at a plurality of bits V-RAMs 15, each of the plurality of V-RAM 15 storing separate display data and the CRT controller retrieving the display data from the at least of the plurality of bit V-RAMs 15; and

operably couple the CRT controller to a plurality of display drivers CRT 19 and PDP 21, each of the plurality of display drivers 19 and 21 writing the separate display data to the plurality of bits V-RAMs (see figures 8, 11A, 11B).

As to claim 38, Zenda '678 teaches a digital storage medium having first display controller 12 coupling to a first display CRT 19, a second display controller 14 coupling to a second display PDP 21 (figure 8).

As to claims 40 and 41, Zenda '678 teaches a digital storage medium having at least two display controller 12 and 14 coupling to one screen memory (V-RAM 15) (figure 8).

9. *As to claim 42*, Zenda '678 teaches a video graphics processing circuit for displaying at least one image on two displays CRT 19 and PDP 31, comprising:

two display CRT controller 12 and PDP 14 included on a single video graphics card (see figure 8);

two CRT driver 19 and PDP driver 21;

V-RAM 15, wherein at least a bit of V-RAM 15 is screen memory, the V-RAM having a plurality of bits, each of bits storing separate display data (see figure 10);

coupling module (gate 55 and gate 57) coupled to two display CRT 19 and PDP 21 and the V-RAM 15;

coupling controller (D-flip flop 59) operably coupled to receive display preferences and to determine whether the display preferences can be fulfilled in observance of configuration properties, the display preferences including at least one of displaying image on more than one of displays, displays separate images on each of the displays, displaying a portion of the image one of the displays and displaying the image on another one of two display CRT 19 and PDP 21, providing different refresh rates for at least two of the displays, providing different resolutions for at least two of displays, selecting one of the displays to display a predetermined type of image, and displaying a first portion of the image on a first one of the displays and displaying a second portion of the image on a second one of the displays;

wherein, when the display preferences can be fulfilled, the D-flip flop provides configuration requirements to the gates 55 and 57, the gates 55 and 57, based on the configuration requirements, operably couples at least one of the two display controller CRT 12 and PDP 14 with at least a portion of the V-RAM 15 and with at least one display, a respective display driver of the two display driver CRT 19 and PDP 21 thereby writing respective separate display data to a respective one of the plurality of bits V-RAM 15, and wherein the at least one of two display controller CRT 12 and PDP 14 retrieves display data from the at least a bit of the V-RAM 15 and provides the display data to the at least one display, and wherein the D-flip flop 59 when the display preferences cannot be fulfilled but a current configuration of two display controllers CRT

12 and PDP 14 to the at least one display can be reconfigured such that the display preferences can be fulfilled while maintaining effective configuration of the current configuration (see figure 8, 11A and 11B).

As to claim 43, Zenda '678 teaches a graphics engine (PD setting control circuit 29 and CRT controller 25) coupling to at least one CRT controller 12 and at least one of the CRT driver 19 (figure 8).

As to claim 44, Zenda '678 teaches a keyboard 16 (user interface, figure 8).

As to claim 45, Zenda '678 teaches BIOS ROM 17, set-up RAM 24 comprising properties memory (CRT pallet data buffer 5 and PDP pallet data buffer 7) that stores configuration properties of two CRT and PDP controllers 12 and 14 and the at least one CRT display 19, wherein the configuration properties include at least one of: limitations of two CRT and PDP controllers 12 and 14 and the at least one CRT display 19 and operational rules of the two CRT and PDP controller 12 and 14 and the at least one CRT display 19 (figure 8).

As to claim 46, Zenda '678 teaches a video graphics processing circuit having first display controller 12 coupling to a first display CRT 19, a second display controller 14 coupling to a second display PDP 21 (figure 8).

As to claim 48, Zenda '678 teaches a video graphics processing circuit having a first controller 12 and a second controller 14 to one V-RAM 15 (figure 8).

10. *As to claim 49*, Zenda '678 teaches a video graphics processing apparatus having V-RAM 15, two CRT controller 12 and PDP controller 14, two display CRT driver

19 and PDP driver 21, a gate 55 and a gate 57 (coupling module), D-flip flop 59 (coupling controller) (figure 8).

As to claim 50, Zenda '678 teaches a graphics engine (PD setting control circuit 29, and CRT controller 25) coupling to plurality of V-RAM 15 (figure 8).

As to claim 51, Zenda 678 teaches a user interface 16.

As to claim 52, Zenda '678 teaches a V-RAM 15 having display refresh rate, display resolution, and type of display (figure 8).

As to claim 56, Zenda '678 teaches the configuration properties comprises means for causing the D-flip flop to couple a first bit V-Ram to more than one of two CRT and PDP controller 12 and 14 (figure 8).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 30, 39, 47 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zenda '678 in view of Zenda (US 5,559,525) hereinafter Zenda '525.

As to claims 30, 39 and 47, Zenda '678 teach all of the claimed limitations of claims 24, 33 and 42, except for "the first display controller couples to a third display." However, Zenda '525 teaches a related video graphics processing circuit which includes a first display controller (87) coupling a third color CRT (107) (see figure 3A). It would have been obvious to a person of ordinary skill in the art at the time of the invention to

utilize the first display controller (87) coupling a color CRT (107) taught by Zenda '525 in Zenda '678's video graphics processing circuit because this would provide capable of selectively different kinds of display device (column 1, lines 11-14 of Zenda '525).

As to claim 53, Zenda '525 teaches a coupling controller (97, 99, 101) to couple a first display controller 87 to a first LCD 91 and a second CRT 107 (figure 3A).

Allowable Subject Matter

13. Claim 54 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: Caine (US 5,361,078) teaches a first display driver 24A couples a first memory 22A and a second display driver 24B couples to a second memory 22B (figure 1). Caine fails to teach "the coupling controller couples a first display driver to a first and a second screen memory portion," recited in claim 54.

Response to Arguments

15. Applicant's arguments with respect to claims 24, 29-33, 38-53 and 56 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Examiner
Art Unit 2674

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600